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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/672,223	09/27/2000	Yun-Sang Lee	AB-1043 US	6183

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EXAMINER	
CHAUDRY, MUJTABA M	

ART UNIT	PAPER NUMBER
2133	16

DATE MAILED: 03/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/672,223	LEE, YUN-SANG	
	Examiner	Art Unit	
	Mujtaba K Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,14-16 and 18-20* is/are pending in the application.

4a) Of the above claim(s) *13 and 17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,14-16 and 18-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The corrected or substitute drawings received on September 27, 2000. These drawings are accepted.

Specification

The corrected or substitute specification received on September 27, 2000. The specification is accepted.

Response to Amendment

Applicant's arguments/amendments with respect to amended claims 1-4 and 16, and previously presented claims 5-12, 14, 15 and 18-20 filed December 15, 2003 have been fully considered but are not persuasive. As a note of reference, claims 13 and 17 have been cancelled, see paper No. 13.

Applicant contends, "...Surlekar (prior art of record) fails to disclose the internal signals to control internal operations of the integrated circuit." The Examiner disagrees. Surlekar teaches (abstract) that the design for testability (DFT) techniques used in dynamic random access memories reduce the time required testing use parallel read/write procedures and similar techniques. The technique of Surlekar compares actual data signal output with an expected data signal in parallel resulting in a faster determination of the memory status. The additional apparatus is incorporated in the memory unit in the vicinity of the group of storage cells under

test. By appropriate selection of the location and function of the apparatus, the test apparatus can result in a smaller chip size, faster processing operation, and lower power consumption. The DFT technique reduces the time for testing by incorporating parallel read/write procedures along with additional test procedures. In particular, Surlekar teaches (Figure 1 and col. 1, lines 14-59) a block diagram of a semiconductor memory unit. In the memory unit, ADDRESS SIGNALs are applied to row address buffers 11 and to column address buffers 12. The ADDRESS SIGNALs stored in the row address buffers 11 are applied to the row decode unit 13 and to the timing and control unit 19, while the ADDRESS SIGNALs stored in the column address buffers are applied to the column decode unit 14 and to the data input/output buffers 16. The signals from the row decode unit 13 and the column decode unit 14 are applied to the memory array 15, the signals applied to the memory array 15 specifying a group of memory array cells to be manipulated in response to control signals. **Control signals are applied to the timing and control circuit 19.** Output signals from the timing and control unit 19 are applied to the data input/output buffers 16. The memory array unit 15 applies signals to, and receives signals from, the data input/output buffers 16. The data input/output buffers 16 receive signals from the data in register 18 and applies signals to the data out register 17. DATA SIGNALs are applied to the data in register and are received from the data out register 17.

Applicant contends, "Surlekar fails to disclose data output buffer for transferring internal integrated circuit signals externally through data input/output pads wherein the internal signals are used for addressing storage locations and for controlling internal operations of the integrated circuit." The Examiner disagrees. In view of above comments and Figure 1, Surlekar teaches data input/output buffers 16. Furthermore, Surlekar teaches (col. 1, lines 28-29), "...control

signals are applied to the timing and control circuit." The Examiner would like to point out that the same control signals that are being applied to the timing and control circuit are being applied to the row decode and column decode units, which are used to address storage locations and controlling internal operations of the integrated circuit.

Applicant contend, "Surlekar fails to disclose a selection circuit for receiving internal signals in response to selection signals corresponding to test information signals where the internal signals are used for addressing storage locations and controlling internal operations." The Examiner disagrees. Surlekar teaches (Figure 3) the selection of one of the addressed storage cells in each quadrant (i.e., shown by the x's in FIG. 2A) is illustrated. Each addressed storage cell is coupled to a sense amplifier 31-34. The output signals from the sense amplifiers 31-34 are applied to selection circuit 35. In response to a SELECT LOCAL INPUT/OUTPUT AMPLIFIER SIGNAL, the DATA SIGNAL from one of the sense amplifiers 31-34 is applied to a predetermined data line 36.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1-12, 14-16 and 18-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Surlekar (USPN 5668764).

The Examiner disagrees with the Applicant and maintains rejections with respect to amended claims 1-4 and 16, and previously presented claims 5-12, 14, 15 and 18-20. All arguments have been considered. It is the Examiner's conclusion that amended claims 1-4 and 16, and previously presented claims 5-12, 14, 15 and 18-20 are not patentably distinct or non-obvious over the prior art of record. See paper No. 8.

Conclusion

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 703-305-7755. The examiner may normally be reached Mon – Thur 7:30 am to 4:30 pm and every other Fri 8:00 am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 703-305-9595. The fax phone number for the organization where this application is assigned is 703-746-7239.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the receptionist at 703-305-3900.

Mujtaba Chaudry
Art Unit 2133
February 23, 2004

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100